IN THE CLAIMS

1. (Previously presented) A phase locked loop (PLL) system including

a phase frequency detector (PFD),

a filter, a variable frequency oscillator (VFO), and

a feedback loop including a frequency divider that has several divider values, said PLL operating over a frequency range that includes a number of frequency sub-ranges, the center frequency of each sub-range being determined by one of said divider values,

said VFO having a variable gain profile, the gain profile of said VFO being controlled by gain control logic which sets the gain profile of said VFO so that the gain of the VFO remains within a desired range as the operation of said PLL moves between said frequency sub-ranges.

2. (Previously presented) A method of operating a phase locked loop (PLL) which operates over a frequency range that includes a number of frequency sub-ranges, said sub-ranges being established by the value of a frequency divider in a feedback loop,

said PLL including a variable frequency oscillator (VFO) the gain profile of which is variable in response to changing the value of selected components of said VFO,

said method including,

determining the particular setting of said selected components for each frequency sub-range that produces a selected gain profile that is within pre-established limits for each of said frequency sub-ranges, and

changing the settings of said selected components to the particular settings for each frequency sub-range when said PLL is set to operate within a particular sub-range.

3. (Previously presented) A phase locked loop(PLL) system including

a phase frequency detector (PFD),

a filter, a variable frequency oscillator (VFO),

and a feedback loop including a frequency divider having a plurality of divide values,

said PLL operating over a frequency range that includes a plurality of frequency sub-ranges, each range being established by a divider value of said divider,

said VFO having variable gain profile, said variable gain profile having one value for each particular frequency sub-range which maintains the gain of said VFO within pre-established limits within said particular frequency sub-range, and

a logic circuit operable when the frequency of operation of said PLL changes frequency sub-range to change the gain profile of said VFO to a value which maintains said gain within pre-established limits over said frequency sub-range.

4. (Original) The system recited in claim 1 wherein said frequency range is from 2.4 GHz to 2.48 GHz.

5. (Previously presented) The method in recited in claim 2 wherein said frequency range is from 2.4 GHz to 2.48 GHz.

6. (Original) The system of claim 1 wherein said desired range of gain is from 0.26GHz per volt to 0.325 GHz per volt.

7. (Original) The method of claim 2 wherein said pre-established limits are from 0.26GHz per volt to 0.325 GHz per volt.

8. (Original) The system in claim 1 wherein said frequency range is divided into three sub-ranges.

9. (Original) The method of claim 2 wherein said frequency range is divided into three sub-ranges.

10. (Previously presented) A phase locked loop(PLL) including

a phase frequency detector (PFD),

a filter, a voltage controlled oscillator (VCO), and

a feedback loop including a frequency divider, said frequency divider having a plurality of divider values,

said PLL operating over a frequency range that includes a number of frequency sub-ranges, said VCO having a variable gain profile, and

means for changing the gain profile of said VCO when said, PLL changes operation between said frequency sub-ranges,

whereby the gain of said VCO is within pre-established limits over each frequency sub-range.

11. (Previously presented) A method of operating a phase locked loop (PLL) which operates over a frequency range that includes a number of frequency sub-ranges, said PLL including a voltage controlled oscillator (VCO) the gain profile of which is variable, said method including:

a feedback loop having a frequency divider, said divider having a plurality of divider values that establish different frequency sub-ranges,

changing the frequency of operation of said PLL,

determining if said PLL is operating in a different frequency sub-range when the frequency of operation changes, and

when the frequency of operation of said PLL changes frequency sub-ranges, changing the gain profile of said VCO to a profile that is within pre-established limits over said frequency sub-range.

12. (Previously presented) A phase locked loop (PLL) system which operates over a frequency range that includes a number of frequency sub-ranges established by the division provided by a frequency divider in a feedback loop, said PLL including

a variable frequency oscillator (VFO) the gain profile of which is variable,

a first circuit for changing the frequency of operation of said PLL,

a second circuit for determining if changes to the frequency of operation of said PLL has changed the frequency sub-range in which said PLL is operating, and

a third circuit operable when the frequency of operation of said PLL changes frequency sub-ranges to change the gain profile of said VFO to a profile that has a gain within pre-established limits over said frequency sub-range.

13. (Original) The system recited in claim 12 wherein said frequency range is from 2.4 Ghz to 2.48 Ghz.

14. (Original) The system of claim 1 wherein said pre-established limits of gain is from 0.26GHz per volt to 0.325 GHz per volt.

15. (Currently amended) A method of operating a phase locked loop (PLL) which operates over a frequency range that includes a number of frequency sub-ranges, said frequency ranges being established by the value of a frequency divider in a feedback loop, said PLL including a variable frequency oscillator (VFO), said PLL having a loop gain profile which is variable, said method including,

determining if changes to the frequency of operation of said PLL has changed the frequency sub-range in which said PLL is operating, and

changing ~~change~~ the loop gain profile of said PLL when the operation of said PLL changes sub-ranges, said profile being changed to a profile that has a gain within pre-established limits over said frequency sub-range.

16. (Original) A phase locked loop (PLL) system recited in claim 12 wherein said third means includes gain control logic which changes the gain of said VFO when said PLL changes sub-ranges.

17. (Original) A phase locked loop (PLL) system recited in claim 12 wherein the overall gain of said system is substantially symmetrical around the center of said frequency range.

18. (Previously presented) A phase locked loop(PLL) system including

a phase frequency detector (PFD),

a filter,

a variable frequency oscillator (VFO), and

a feedback loop including a frequency divider, which has a plurality of divider values, thereby establishing a plurality of frequency sub-ranges,

said PLL operating over a frequency range that includes a number of said frequency sub-ranges,

said PLL having a variable loop gain profile,

the loop gain profile of said PLL being controlled by gain profile control logic which sets the loop gain profile of said PLL so that the loop gain of the said PLL remains within a desired range as the operation of said PLL moves between said frequency sub-ranges.

19. (Original) The phase locked loop system recited in claim 18 wherein said loop gain profile is changed by changing the gain profile of said VFO.

20. (Original) The phase locked loop system recited in claim 18 wherein said VFO is a Voltage controlled oscillator (VCO).